



## TE0711 Test Board

Revision v.9

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Online version of this document:

<https://wiki.trenz-electronic.de/display/PD/TE0711+Test+Board>

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## 4 Overview

Simple MicroBlaze Design with Hello TE0711 and LED control via VIO. Refer to <http://trenz.org/te0711-info> for the current online version of this manual and other available documentation.

### 4.1 Key Features

- Vitis/Vivado 2019.2
- MicroBlaze
- LED
- QSPI
- UART

### 4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2020-09-01	2019.2	TE0711-test_board-vivado_2019.2-build_14_20200901073500.zip TE0711-test_board_noprebuilt-vivado_2019.2-build_14_20200901073630.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• 2019.2 update</li> </ul>
2017-12-07	2017.2	TE0711-test_board_noprebuilt-vivado_2017.2-build_05_20171207122944.zip TE0711-test_board-vivado_2017.2-build_05_20171207122644.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• initial release</li> </ul>

**Table 1: Design Revision History**

### 4.3 Release Notes and Known Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

**Table 2: Known Issues**

## 4.4 Requirements

### 4.4.1 Software

Software	Version	Note
Vitis	2019.2	needed, Vivado is included into Vitis installation

**Table 3: Software**

### 4.4.2 Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).<sup>1</sup>

Complete List is available on <design name>/board\_files/\*\_board\_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0711-01-35-2C	35_2c	REV01	NA	32MB	NA	NA	NA
TE0711-01-100-2C	100_2c	REV01	NA	32MB	NA	NA	NA
TE0711-01-35-2I	35_2i	REV01	NA	32MB	NA	NA	NA
TE0711-01-100-2I	100_2i	REV01	NA	32MB	NA	NA	NA

**Table 4: Hardware Modules**

Design supports following carriers:

Carrier Model	Notes
TE0701	<ul style="list-style-type: none"> <li>See restrictions on usage with 7 Series Carriers: <a href="#">4 x 5 SoM Carriers</a><sup>2</sup></li> </ul>

<sup>1</sup> <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>

<sup>2</sup> <https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers>

Carrier Model	Notes
TE0703	<ul style="list-style-type: none"> <li>See restrictions on usage with 7 Series Carriers: <a href="#">4 x 5 SoM Carriers</a><sup>3</sup></li> <li>Used as reference carrier.</li> </ul>
TE0705	<ul style="list-style-type: none"> <li>See restrictions on usage with 7 Series Carriers: <a href="#">4 x 5 SoM Carriers</a><sup>4</sup></li> </ul>
TE0706	<ul style="list-style-type: none"> <li>See restrictions on usage with 7 Series Carriers: <a href="#">4 x 5 SoM Carriers</a><sup>5</sup></li> </ul>
TEBA0841	<ul style="list-style-type: none"> <li>See restrictions on usage with 7 Series Carriers: <a href="#">4 x 5 SoM Carriers</a><sup>6</sup></li> <li>No SD Slot available, pins goes to Pin Header</li> </ul>

**Table 5: Hardware Carrier**

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct typ
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI

**Table 6: Additional Hardware**

## 4.5 Content

For general structure and of the reference design, see [Project Delivery - Xilinx devices](#)<sup>7</sup>

### 4.5.1 Design Sources

Type	Location	Notes
Vivado	<design name>/ block_design <design name>/ constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts

<sup>3</sup> <https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers>

<sup>4</sup> <https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers>

<sup>5</sup> <https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers>

<sup>6</sup> <https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers>

<sup>7</sup> <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices>



Type	Location	Notes
Vitis	<design name>/sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

**Table 7: Design sources**

#### 4.5.2 Additional Sources

Type	Location	Notes
--	--	--

**Table 8: Additional design sources**

#### 4.5.3 Prebuilt

File	File-Extension	Description
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.xsa	Exported Vivado Hardware Specification for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
MCS-File	*.mcs	Flash Configuration File with Boot-Image (MicroBlaze or FPGA part only)
MMI-File	*.mmi	File with BRAM-Location to generate MCS or BIT-File with *.elf content (MicroBlaze only)

File	File-Extension	Description
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

**Table 9: Prebuilt files (only on ZIP with prebuilt content)**

#### 4.5.4 Download

---

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- [TE0711 "Test Board" Reference Design Download Area](https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/TE0711/Reference_Design/2019.2/test_board)<sup>8</sup>

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<sup>8</sup> [https://shop.trenz-electronic.de/Download/?path=Trenz\\_Electronic/Modules\\_and\\_Module\\_Carriers/4x5/TE0711/Reference\\_Design/2019.2/test\\_board](https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/TE0711/Reference_Design/2019.2/test_board)

## 5 Design Flow

**!** Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- [Xilinx Development Tools](#)<sup>9</sup>
- [Vivado Projects - TE Reference Design](#)<sup>10</sup>
- [Project Delivery](#).<sup>11</sup>

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "\_create\_win\_setup.cmd" on Windows OS and "\_create\_linux\_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also be executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)<sup>12</sup>

1. \_create\_win\_setup.cmd/\_create\_linux\_setup.sh and follow instructions on shell:

```

B:\Design\cores\2017.2\design\TE0711\test_board>setlocal
-----Set design paths-----
-- Run Design with: _create_win_setup
-- Use Design Path: B:\Design\cores\2017.2\design\TE0711\test_board\
-----TE Reference Design-----
-- (c) Go to CMD-File Generation (Manual setup)
-- (d) Go to Documentation (Web Documentation)
-- (x) Exit Batch (nothing is done!)
-- (0) Create minimum setup of CMD-Files and exit Batch
-- (1) Create maximum setup of CMD-Files and exit Batch
-----
Select (ex.: '0' for min setup):
  
```

2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x: \<design name>)
4. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process
  - a. (optional for manual changes) Select correct device and Xilinx install path on "design\_basic\_settings.cmd" and create Vivado project with "vivado\_create\_project\_guiemode.cmd"
 

Note: Select correct one, see also [TE Board Part Files](#)<sup>13</sup>
5. Create XSA and export to prebuilt folder
  - a. Run on Vivado TCL: TE::hw\_build\_design -export\_prebuilt
 

Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Generate ApplicationFiles with Vitis

<sup>9</sup> <https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftware-BasicUserGuides>

<sup>10</sup> <https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design>

<sup>11</sup> <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices>

<sup>12</sup> <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDeliveryXilinxdevices-Currentlylimitationsoffunctionality>

<sup>13</sup> <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>

- a. Run on Vivado TCL: `TE::sw_run_vitis -all`  
Note: Scripts generate applications and bootable files, which are defined in "sw\_lib/apps\_list.csv"
  - b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: `TE::sw_run_vitis`  
Note: TCL scripts generate also platform project, this must be done manually in case GUI is used. See [Vitis](#)<sup>14</sup>
7. Copy Application (hello\_te0711.elf) into \firmware\microblaze\_0\
8. Regenerate Design:
  - a. Run on Vivado TCL: `TE::hw_build_design -export_prebuilt`  
Note: App from Firmware folder will be add into BlockRAM. If you add other app, you must select \*.elf manually on Vivado
  - b. (alternative) Use SDK or Vivado to update generate Bitfile with new Application and regenerate mcs manually.

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<sup>14</sup> <https://wiki.trenz-electronic.de/display/PD/Vitis>

## 6 Launch

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### 6.1 Programming

---

 Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: [Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging](#)<sup>15</sup>

#### 6.1.1 Get prebuilt boot binaries

---

1. `_create_win_setup.cmd/_create_linux_setup.sh` and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
  - a. Select assembly version
  - b. Validate selection
  - c. Select Create and open delivery binary folder  
Note: Folder (`<project folder>/_binaries_<Artikel Name>`) with subfolder (`boot_<app name>`) for different applications will be generated

#### 6.1.2 QSPI

---

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "`vivado_open_existing_project_gui_mode.cmd`" or if not created, create with "`vivado_create_project_gui_mode.cmd`"
3. Type on Vivado TCL Console: `TE::pr_program_flash -swapp hello_te0711`
4. Reboot (if not done automatically)

#### 6.1.3 SD

---

Not used on this Example.

#### 6.1.4 JTAG

---

- Open Vivado HW Manager with
- Program FPGA with Bitstream

### 6.2 Usage

---

1. Prepare HW like described on section [Programming](#)(see page 13)
2. Connect UART USB (most cases same as JTAG)
3. Power On PCB  
Note: FPGA Loads Bitfile from Flash

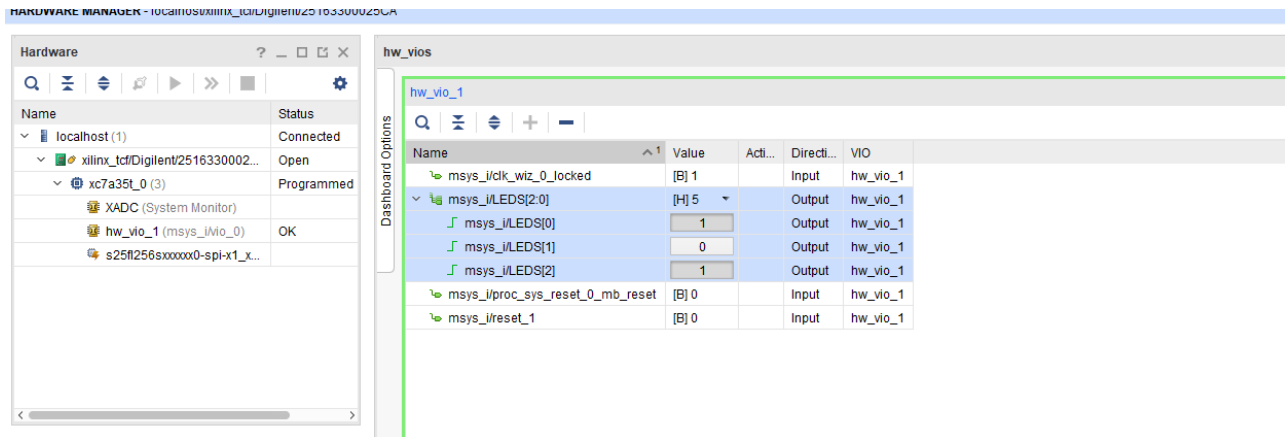
---

<sup>15</sup> <https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftwareProgrammingandDebugging>

## 6.2.1 Vivado HW Manager

1. Open Vivado HW-Manager and add VIO signal to dashboard (\*.ltx located on prebuilt folder)
  - a. Select LEDs and set to Toggle Button

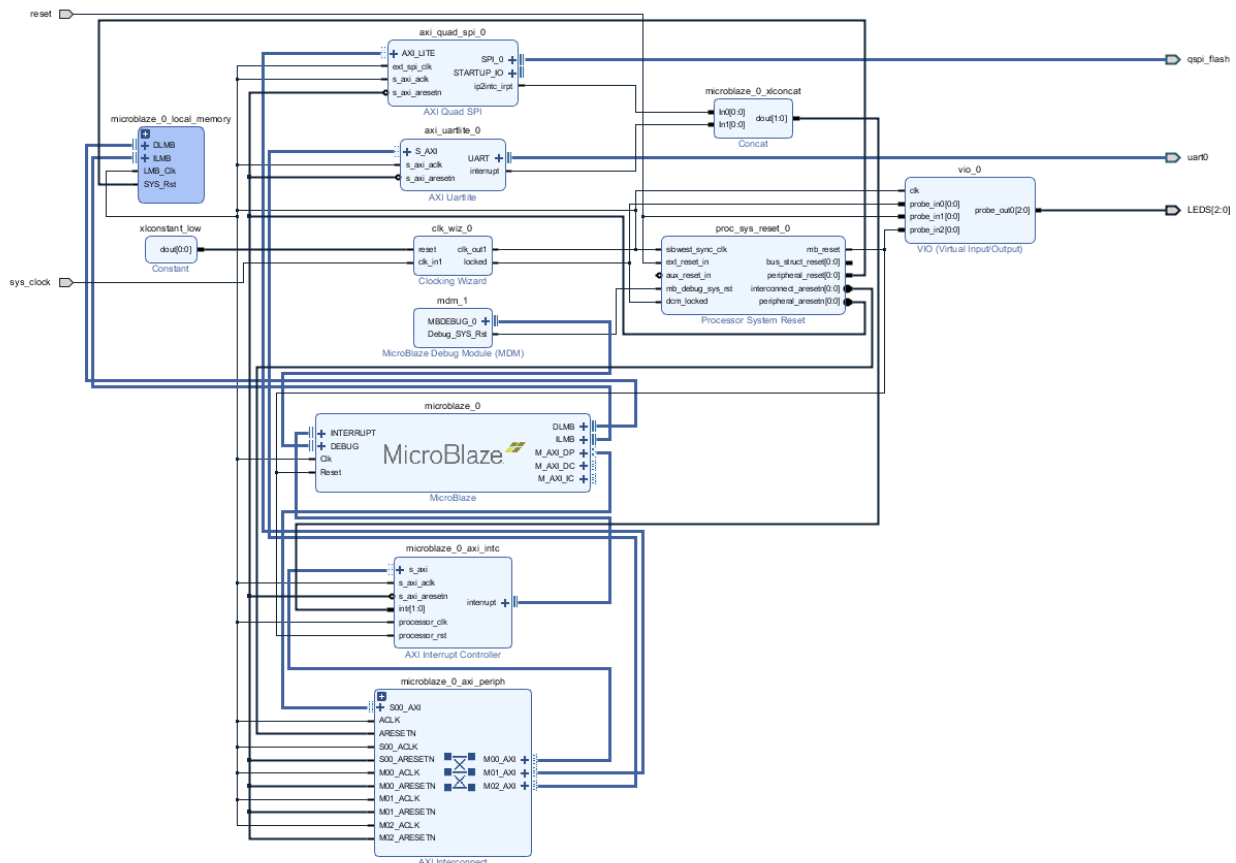
Note: LEDS[0]=D1, LEDS[1]=D2, LEDS[2]=D3 on PCB. LEDS[2] is inverted on PCB.



**Figure 1: Vivado Hardware Manager**

## 7 System Design - Vivado

### 7.1 Block Design



**Figure 2: Block Design**

### 7.2 Constrains

#### 7.2.1 Basic module constrains

##### \_i\_bitgen\_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 66 [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCC0 [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.M1PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M2PIN PULLNONE [current_design]
```

```
set_property BITSTREAM.CONFIG.M0PIN PULLNONE [current_design]  
set_property BITSTREAM.CONFIG.USR_ACCESS_TIMESTAMP [current_design]
```

#### **\_i\_bitgen.xdc**

```
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLDOWN [current_design]
```

## 7.2.2 Design specific constrain

#### **\_i\_io.xdc**

```
set_property PACKAGE_PIN A8 [get_ports {LEDS[0]}]  
set_property PACKAGE_PIN L15 [get_ports {LEDS[1]}]  
set_property PACKAGE_PIN R17 [get_ports {LEDS[2]}]  
set_property IOSTANDARD LVCMOS18 [get_ports {LEDS[0]}]  
set_property IOSTANDARD LVCMOS33 [get_ports {LEDS[1]}]  
set_property IOSTANDARD LVCMOS33 [get_ports {LEDS[2]}]  
set_property PULLDOWN true [get_ports reset]
```



## 8 Software Design - Vitis

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For SDK project creation, follow instructions from:

[Vitis](#)<sup>16</sup>

### 8.1 Application

---

Template location: `./sw_lib/sw_apps/`

#### 8.1.1 hello\_te0711

---

Hello TE0711 is a Xilinx Hello World example as endless loop instead of one console output.

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<sup>16</sup> <https://wiki.trenz-electronic.de/display/PD/Vitis>

## 9 Additional Software


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No additional software is needed.

## 10 Appx. A: Change History and Legal Notices

### 10.1 Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
 2020-09-02	v.9(see page 6)	@ John Hartfiel <sup>17</sup>	<ul style="list-style-type: none"> <li>• 2019.2 release</li> <li>• Docu update</li> </ul>
2018-11-30	v.8	John Hartfiel	<ul style="list-style-type: none"> <li>• correction download link</li> </ul>
2017-12-07	v.7	John Hartfiel	<ul style="list-style-type: none"> <li>• 2017.2 release</li> </ul>
	All	@ John Hartfiel <sup>18</sup>	

### 10.2 Legal Notices

### 10.3 Data Privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

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<sup>17</sup> <https://wiki.trenz-electronic.de/display/~j.hartfiel>

<sup>18</sup> <https://wiki.trenz-electronic.de/display/~j.hartfiel>

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## 10.8 Environmental Protection

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To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

## 10.9 REACH, RoHS and WEEE

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### REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of [REACH](http://guidance.echa.europa.eu/)<sup>19</sup>. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no [SVHC \(Substances of Very High Concern\) on the Candidate List](https://echa.europa.eu/candidate-list-table)<sup>20</sup> are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the [European Chemicals Agency \(ECHA\)](http://www.echa.europa.eu/)<sup>21</sup>.

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Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

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Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is

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<sup>19</sup> <http://guidance.echa.europa.eu/>

<sup>20</sup> <https://echa.europa.eu/candidate-list-table>

<sup>21</sup> <http://www.echa.europa.eu/>

necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

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